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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,598	08/30/2001	Gary L. Swoboda	TI-30480	2621

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,598	SWOBODA ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 29 have been examined. Claims 1 - 29 have been rejected.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 16, 17, 18, 19, 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Edwards065 (U.S. Patent 6,918,065).

a. **Regarding claim 1**, Edwards065 teaches:

i. a method of providing emulation information indicative of internal operations of a data processor for use by an apparatus external to the data processor **(figure 1, all elements, element 103 is the apparatus; and figure 7; and figure 8; and column 7, lines 45 - 50; and column 2, lines 9 - 67)**.

ii. providing a stream of emulation trace information indicative of data processing operations performed by the data processor **(figure 2, elements 221, 102, and 103; and column 2, lines 9 - 67)**.

iii. providing a stream of timing information indicative of operation of a clock used by the data to perform data processing operations **(figure 2, elements 218, 102, and 103; and column 7, lines 27 - 33)**.

iv. inserting in the trace stream and in the timing stream information indicative of a temporal relationship between the trace information and the timing information **(figure 2, elements 218, 216, 217, 205, 221, 203, 204, 202; and column 23, lines 23 - 30; and column 13, Table 1, field "Timestamp"; and column 23, Table 7, field "Time Value";**

and Figure 7,especially element 708; please note that the timestamp and time fields of the trace messages would have been information indicative of a temporal relationship between the trace information and the timing information).

b. **Regarding claim 16,** Edwards065 teaches:

i. That trace information includes memory reference information indicative of a memory access associated with the data processing operations **(column 15, Table 3, "Operand Address Watchpoint Trace Message").**

c. **Regarding claim 17,** Edwards065 teaches:

i. The trace information includes program counter values associated with the data processing operations **(figure 7, element 710; columns 12 and 13, Table 1, field "PC");**

d. **Regarding claims 18 and 25,** Edwards065 teaches:

i. A combiner coupled to the trace generator and the timing generator for combining the trace stream and the timing stream into a composite stream **(figure 2, element 205; and column 8, lines 5 - 50).**

e. **Regarding claim 19,** Edwards065 teaches:

i. an apparatus for providing emulation information indicative of internal operations of a data processor for use by an apparatus external to the data processor **(figure 1, all elements, element 103 is the apparatus; and figure 7; and figure 8; and column 7, lines 45 - 50; and column 2, lines 9 - 67).**

ii. A first input for coupling to the data processor **(figure 2, elements 221, 102, and 103).**

iii. A trace generator coupled to said first input for providing a stream of emulation trace information indicative of data processing operations performed by the data processor **(figure 2, elements 221, 102, and 103).**

iv. A second input for coupling to the data processor **(figure 2, elements 218, 102, and 103).**

v. A timing generator coupled to said second input for providing a stream of timing information indicative of operation of a clock used by the data processor to perform data processing operations **(figure 2, elements 218, 102, and 103).**

vi. Said trace generator and said timing generator cooperable for inserting into the trace stream and the timing stream information indicative of a temporal relationship between the trace information and the timing information **(figure 2, elements 218, 216, 217, 205, 221, 203, 204, 202; and column 7, lines 27 - 33; and column 23, lines 23 - 30; and**

column 13, Table 1, field "Timestamp"; and column 23, Table 7, field "Time Value"; and Figure 7,especially element 708; please note that the timestamp and time fields of the trace messages would have been information indicative of a temporal relationship between the trace information and the timing information).

f. **Regarding claim 26,** Edwards065 teaches:

i. an integrated circuit **(figure 1, element 101).**

ii. a data processor for performing data processing operations **(figure 1, element 102);**

iii. an apparatus coupled to said data processor for providing emulation information indicative of said data processing operations to an emulation apparatus located externally of said integrated circuit **(figure 2, elements 102 and 103),** including a trace generator for providing a stream of emulation trace information indicative of said data processing operations **(figure 2, elements 102, 221),** and a timing generator for providing a stream of timing information indicative of operation of a clock used by said data processor to perform said data processing operations **(figure 2, elements 102, 218);** and

iv. said trace generator and said timing generator cooperable for inserting into the trace stream and the timing stream information indicative of a temporal relationship between the trace information and the timing information **(figure 2, elements 218, 216, 217, 205, 221, 203, 204, 202; and column 7, lines 27 - 33; and column 23, lines 23 - 30; and column 13, Table 1, field "Timestamp"; and column 23, Table 7, field "Time Value"; and Figure 7,especially element 708; please note that the timestamp and time fields of the trace messages would have been information indicative of a temporal relationship between the trace information and the timing information).**

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) in view of Bellamy (Bellamy, Abraham; "Digital Telephony", 1982, John Wiley & Sons).

a. **Regarding claims 2 and 20,** Edwards065 teaches:

i. The timing generator is operable for providing in said timing stream a plurality of bits which are indicative of a cycle of said clock **(figure 2, elements 102 and 218; column 8, lines 34 - 45; and column 13, Table 1, field "Timestamp");**

b. **Regarding claims 2 and 20,** Edwards065 does not specifically teach:

i. The timing generator is operable for providing in said timing stream a plurality of bits which are ***respectively*** indicative of a ***plurality of said cycles*** of said clock

c. **Regarding claims 2 and 20,** Bellamy teaches:

i. Providing a bit map with a plurality of bits which are respectively indicative of a plurality of time slots **(page 372, first paragraph).**

d. The motivation to use the art of Bellamy with the art of Edwards065 would have been the ease of implementation. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Bellamy with the art of Edwards065 to produce the claimed invention.

6. Claims 3 - 15 and 21 - 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) in view of Bellamy (Bellamy, Abraham; "Digital Telephony", 1982, John Wiley & Sons), further in view of Goldrian (Goldrian, G.; Ulland, H.; "Tracing of Large Amounts of Data by Using Main Memory as a Trace Buffer", IBM Technical Disclosure Bulletin, Volume 40, Number 6, June 1997).

a. **Regarding claims 3 and 21,** Edwards065 teaches:

i. said trace generator and said timing generator are cooperable for inserting mutually corresponding identifiers into the trace stream and the timing stream, respectively **(figure 2; and column 22, lines 35 - 55, and column 23, lines 22 - 30; and figure 7, element 708; and column 8, lines 34 - 50; and figure 2; and column 13, Table 1, field "Timestamp"; and column 23, Table 7, field "Time Value").**

b. **Regarding claims 3 and 21,** Edwards065 does not specifically teach:

i. said trace generator and said timing generator are cooperable for inserting mutually corresponding identifiers into the trace stream and the timing stream, respectively, ***one of said trace and timing generators further operable for inserting in its associated stream an index for identifying a bit of the timing stream which represents a***

clock cycle that timewise corresponds to data in the trace stream at a point in the trace stream at which the trace stream identifier is inserted.

c. **Regarding claims 3 and 21,** Goldrian teaches:

i. one of said trace and timing generators further operable for inserting in its associated stream an index for identifying a bit of the timing stream which represents a clock cycle that timewise corresponds to data in the trace stream at a point in the trace stream at which the trace stream identifier is inserted **(page 49, second paragraph).**

d. **Regarding claim 4,** Edwards065 teaches:

i. That inserting the index includes inserting the index into the trace stream **(figure 7, element 708; column 8, lines 34 - 50).**

e. **Regarding claim 5,** Edwards065 teaches:

i. the trace information includes program counter values associated with said data processing operations **(columns 12 and 13, Table 1, field "PC").**

f. **Regarding claims 6 and 22,** Edwards065 teaches:

i. the timing generator is operable for inserting its identifier into the timing stream **(figure 2, elements 102, 218, 216, 217, 205; and column 7, lines 27 - 32).**

g. **Regarding claims 6 and 22,** Edwards065 does not specifically teach:

i. the timing generator is operable *for arranging groups of said bits into respective packets within the timing stream* and for inserting its *associated* identifier into the timing stream *at a predetermined position relative to one of said packets*.

h. **Regarding claims 6 and 22,** Goldrian teaches:

i. arranging groups of said bits into respective packets within the timing stream and for inserting its associated identifier into the timing stream at a predetermined position relative to one of said packets **(page 49, second paragraph; it would have been obvious to have the limitation).**

i. **Regarding claim 7,** Edwards065 does not specifically teach:

i. The method of claim 6, wherein said one packet includes the bit identified by said index.

j. **Regarding claim 7,** Goldrian teaches:

i. that said one packet includes the bit identified by said index **(page 49, second paragraph; it would have been obvious to have said one packet including the bit identified by said index).**

k. **Regarding claim 8,** Edwards065 does not specifically teach:

i. The method of claim 7, wherein said index inserting step includes inserting said index into the trace stream.

l. **Regarding claim 8,** Goldrian teaches:

i. The method of claim 7, wherein said index inserting step includes inserting said index into the trace stream **(page 49, second paragraph; it would have been obvious to have the limitation).**

m. **Regarding claim 9,** Edwards065 does not specifically teach:

i. The method of claim 7, wherein said index identifies a bit position within said one packet occupied by the identified bit.

n. **Regarding claim 9,** Goldrian teaches:

i. the said index identifies a bit position within said one packet occupied by the identified bit **(page 49, second paragraph; it would have been obvious to have the limitation).**

o. **Regarding claim 10,** Edwards065 does not specifically teach:

i. The method of claim 9, wherein said index inserting step includes inserting said index into the trace stream.

p. **Regarding claim 10,** Goldrian teaches:

i. the said index inserting step includes inserting said index into the trace stream **(page 49, second paragraph; it would have been obvious to have the limitation).**

q. **Regarding claim 11,** Edwards065 teaches:

i. Providing a further stream of emulation trace information indicative of data processing operations performed by the data processor, and inserting into the further trace stream an identifier which corresponds to said mutually corresponding identifiers **(figure 2, elements 222, 206, 204, 205; and column 8, lines 27 - 50; it would have been obvious to have the limitation).**

r. **Regarding claim 12,** Edwards065 teaches:

i. The method of claim 11, wherein one of said trace streams includes program counter values associated with said data processing operations **(figure 2, element 221; and figure 7, element 710; columns 12 and 13, Table 1, field "PC"; it would have been obvious to have the limitation)**.

s. **Regarding claim 13**, Edwards065 teaches:

i. The other trace stream includes memory reference information indicative of a memory access associated with said data processing operations **(figure 2, element 221; and columns 18 and 19, Table 7, field "address"; it would have been obvious to have the limitation)**.

t. **Regarding claim 14**, Edwards065 teaches:

i. One of said trace streams includes memory reference information indicative of a memory access associated with said data processing operations **(figure 2, element 221; and columns 18 and 19, Table 7, field "address"; it would have been obvious to have the limitation)**.

u. **Regarding claim 15**, Edwards065 teaches:

i. Combining the trace streams and the timing stream into a single composite stream **(figure 2, elements 218, 216, 217, 205, 221, 203, 204, 205, 202; column 7, lines 27 - 34; it would have been obvious to have the limitation)**.

v. **Regarding claim 23**, Edwards065 teaches:

i. That the packet includes the bit identified by the index **(figure 2, elements 102, 218, 216, 217, 205; and column 7, lines 27 – 32; and column 22, lines 34 - 46)**.

w. **Regarding claim 24**, Edwards065 teaches:

i. Said that the said one generator is the trace generator **(column 8, lines 34 – 50; and column 22, lines 34 - 46)**.

x. The motivation to use the art of Goldrian with the art of Edwards065 would have been the benefit of a method provided to correlate events to microcode routines that initiated or processed the events **(page 49, second paragraph)**. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Goldrian with the art of Edwards065 to produce the claimed inventions.

7. Claims 27 - 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) in view of Miyayama (U.S. Patent 6,665,821).

a. **Regarding claim 27**, Edwards065 teaches:

i. an integrated circuit including a data processor for performing data processing operations **(figure 1, elements 101 and 102)**.

ii. an ***external device*** located externally of said integrated circuit and coupled thereto **(figure 1, elements 101 and 106)**.

iii. said integrated circuit including an apparatus coupled between said data processor and said ***external device*** for providing to said ***external device*** emulation information indicative of said data processing operations **(figure 1, element 103; and figure 2, elements 102, 103, 221)**, said apparatus including a trace generator for providing a stream of emulation trace information indicative of said data processing operations **(figure 2, elements 102, 103, 221; and column 2, lines 10 - 67)**, and a timing generator for providing a stream of timing information indicative of operation of a clock used by said data processor to perform said data processing operations **(figure 2, elements 102, 103, 218)**; and

iv. said trace generator and said timing generator cooperable for inserting into the trace stream and the timing stream information indicative of a temporal relationship between the trace information and the timing information **(figure 2, elements 218, 216, 217, 205, 221, 203, 204, 202; and column 7, lines 27 – 33; and column 23, lines 23 – 30; and column 13, Table 1, field "Timestamp"; and column 23, Table 7, field "Time Value"; and Figure 7,especially element 708; please note that the timestamp and time fields of the trace messages would have been information indicative of a temporal relationship between the trace information and the timing information)**.

b. **Regarding claim 27**, Edwards065 does not specifically teach:

i. an ***emulation controller*** located externally of said integrated circuit and coupled thereto ***for controlling emulation operations of said data processor;***

ii. said integrated circuit including an apparatus coupled between said data processor and said ***emulation controller*** for providing to said ***emulation controller*** emulation information indicative of said data processing operations, said apparatus including a trace generator for providing a stream of emulation trace information indicative of said data processing operations, and a timing generator for providing a

stream of timing information indicative of operation of a clock used by said data processor to perform said data processing operations;

c. **Regarding claim 27**, Miyayama teaches:

i. an emulation controller located externally of said integrated circuit and coupled thereto for controlling emulation operations of said data processor **(figure 1, element 304; and figure 6, elements 10 and 20 and connecting link; and column 1, lines 20 - 35)**;

ii. said integrated circuit and said ***emulation controller*** for providing to an ***emulation controller*** emulation information indicative of said data processing operations **(figure 1, element 304; and column 1, lines 20 - 35)**;

d. **Regarding claim 28**, Miyayama teaches:

i. a man/machine interface coupled to aid emulation controller for permitting a user to communicate with said emulation controller **(figure 1, element "Host System")**.

e. **Regarding claim 29**, Miyayama teaches:

i. the man/machine interface is a visual interface **(figure 1, element "Host System")**.

f. The motivation to combine the art of Miyayama with the art of Edwards065 would have been the benefit recited in Miyayama that the debugging tool can perform various processes necessary for debugging **(column 1, lines 20 - 30)**.

g. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Miyayama with the art of Edwards065 to produce the claimed inventions.

Conclusion

Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul L. Rodriguez 7/21/05
Primary Examiner
Art Unit 2125